

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A multiply-accumulate module
2 comprising:

3 a multiply-accumulate core, wherein said multiply-accumulate
4 core comprises:

5 a plurality of Booth encoder cells;

6 a plurality of Booth decoder cells connected to at least
7 one of said Booth encoder cells; and

8 a plurality of Wallace tree cells connected to at least
9 one of said Booth decoder cells;

10 wherein said multiply-accumulate module includes a plurality
11 of electrical paths which further include at least one critical
12 path, said at least one critical path being an electrical path for
13 which an amount of time that it takes for an electrical signal to
14 travel from an input of said multiply-accumulate core to an output
15 of said multiply-accumulate core is greater than or equal to a
16 predetermined amount of time and less than a longest amount of time
17 that it takes any other electrical signal to travel from said input
18 of said multiply-accumulate core to said output of said multiply-
19 accumulate core, wherein said predetermined amount of time is less
20 than said longest amount of time;

21 said plurality of Booth decoder cells includes at least one
22 first Booth decoder cell and at least one second Booth decoder
23 cell, each of said at least one first Booth decoder cell
24 structurally the same as each of said at least one second Booth
25 decoder cells except that at least one of a first plurality of
26 transistors of said first Booth decoder cell is constructed to have
27 a width greater than a width of a corresponding one of a second
28 plurality of transistors of said second Booth decoder cell;

29 said plurality of Wallace tree cells including at least one
30 first Wallace tree cell and at least one second Wallace tree cell,
31 each of said at least one first Wallace tree cell structurally the
32 same as each of said at least one second Wallace tree cell except
33 that at least one of a first plurality of transistors of said first
34 Wallace tree cell is constructed to have a width greater than a
35 width of a corresponding one a second plurality of transistors of
36 said second Wallace tree cell;

37 wherein said at least one first Wallace tree cell and said at
38 least one first Booth decoder cell are disposed on said at least
39 one critical path; and

40 wherein said at least one second Wallace tree cell and said at
41 least one second Booth decoder cell are disposed on an electrical
42 path not said at least one critical path and are not disposed on
43 any of said at least one critical path.

2. (Canceled)

1 3. (Previously Presented) The multiply-accumulate module of claim
2 1, wherein said multiply-accumulate core further comprises:

3 an adder connected to at least one of said Wallace tree cells;

4 a saturation detector connected to said adder, wherein said
5 multiply-accumulate module further comprises:

6 at least one input register connected to at least one of said
7 Booth encoding cells; and

8 at least one result register connected to said saturation
9 detector.

4 to 9. (Canceled)

1 10. (Previously Presented) A parallel multiplier comprising:
2 a parallel multiplier core, wherein said parallel multiplier
3 core comprises:
4 a plurality of Booth encoder cells;
5 a plurality of Booth decoder cells connected to at least
6 one of said Booth encoder cells; and
7 a plurality of Wallace tree cells connected to at least
8 one of said Booth decoder cells;
9 wherein said parallel multiplier includes a plurality of
10 electrical paths which further include at least one critical path,
11 said at least one critical path being an electrical path for which
12 an amount of time that it takes for an electrical signal to travel
13 from an input of said parallel multiplier core to an output of said
14 parallel multiplier core is greater than or equal to a
15 predetermined amount of time and less than a longest amount of time
16 that it takes any other electrical signal to travel from said input
17 of said parallel multiplier core to said output of said parallel
18 multiplier core, wherein said predetermined amount of time is less
19 than said longest amount of time;
20 said plurality of Booth decoder cells includes at least one
21 first Booth decoder cell and at least one second Booth decoder
22 cell, each of said at least one first Booth decoder cell
23 structurally the same as each of said at least one second Booth
24 decoder cells except that at least one of a first plurality of
25 transistors of said first Booth decoder cell is constructed to have
26 a width greater than a width of a corresponding one of a second
27 plurality of transistors of said second Booth decoder cell;
28 said plurality of Wallace tree cells including at least one
29 first Wallace tree cell and at least one second Wallace tree cell,
30 each of said at least one first Wallace tree cell structurally the
31 same as each of said at least one second Wallace tree cell except
32 that at least one of a first plurality of transistors of said first

33 Wallace tree cell is constructed to have a width greater than a
34 width of a corresponding one a second plurality of transistors of
35 said second Wallace tree cell;

36 wherein said at least one first Wallace tree cell and said at
37 least one first Booth decoder cell are disposed on said at least
38 one critical path; and

39 wherein said at least one second Wallace tree cell and said at
40 least one second Booth decoder cell are disposed on an electrical
41 path not said at least one critical path and are not disposed on
42 any of said at least one critical path.

11. (Canceled)

1 12. (Previously Presented) The parallel multiplier of claim 10,
2 wherein said parallel multiplier core further comprises:

3 an adder connected to at least one of said Wallace tree cells;
4 a saturation detector connected to said adder, wherein said
5 parallel multiplier further comprises:

6 at least one input register connected to at least one of said
7 Booth encoding cells; and

8 at least one result register connected to said saturation
9 detector and at least one of said Wallace tree cells.

13 to 18. (Canceled)

1 19. (Previously Presented) A method of designing a multiply-
2 accumulate module comprising the steps of:

3 providing a multiply-accumulate core, wherein the step of
4 providing a multiply-accumulate core comprises the steps of:

5 providing a plurality of Booth encoder cells;

6 connecting a plurality of Booth decoder cells to at least
7 one of said Booth encoder cells;

8 connecting a plurality of Wallace tree cells to at least
9 one of said Booth decoder cells;
10 defining a predetermined amount of time greater than zero
11 and less than a longest amount of time that it takes any electrical
12 signal to travel from said input of said multiply-accumulate core
13 to said output of said multiply-accumulate core;
14 defining at least one critical path within said multiply-
15 accumulate module, said at least one critical path being an
16 electrical path for which an amount of time that it takes for an
17 electrical signal to travel from an input of said multiply-
18 accumulate core to an output of said multiply-accumulate core is
19 greater than or equal to said predetermined amount of time and less
20 than said longest amount of time ;
21 defining a first Wallace tree cell and a second Wallace
22 tree cell, each of said first Wallace tree cell structurally the
23 same as each of said second Wallace tree cell except that at least
24 one of a first plurality of transistors of said first Wallace tree
25 cell is constructed to have a width greater than a width of a
26 corresponding one a second plurality of transistors of said second
27 Wallace tree cell;
28 defining a first Booth decoder cell and a second Booth
29 decoder cell, each of said first Booth decoder cell structurally
30 the each of same as said second Booth decoder cell except that at
31 least one of a first plurality of transistors of said first Booth
32 decoder cell is constructed to have a width greater than a width of
33 a corresponding one of a second plurality of transistors of said
34 second Booth decoder cell;
35 disposing at least one first Wallace tree cell and at
36 least one first Booth decoder cell on said at least one critical
37 path;

38 disposing at least one second Wallace tree cell and said
39 at least one second Booth decoder cell are on an electrical path
40 not said at least one critical path; and
41 not disposing any second Wallace tree cell or any second
42 Booth decoder cell on any of said at least one critical path.

1 20. (Previously Presented) A method of designing a parallel
2 multiplier comprising the steps of:
3 providing a parallel multiplier core, wherein the step of
4 providing a parallel multiplier core comprises the steps of:
5 providing a plurality of Booth encoder cells;
6 connecting a plurality of Booth decoder cells to at least
7 one of said Booth encoder cells;
8 connecting a plurality of Wallace tree cells to at least
9 one of said Booth decoder cells;
10 defining a predetermined amount of time greater than zero
11 and less than a longest amount of time that it takes any electrical
12 signal to travel from said input of said parallel multiplier core
13 to said output of said parallel multiplier core;
14 defining at least one critical path within said parallel
15 multiplier, said at least one critical path being an electrical
16 path for which an amount of time that it takes for an electrical
17 signal to travel from an input of said parallel multiplier core to
18 an output of said parallel multiplier core is greater than or equal
19 to said predetermined amount of time and less than said longest
20 amount of time;
21 defining a first Wallace tree cell and a second Wallace
22 tree cell, each of said first Wallace tree cell structurally the
23 same as each of said second Wallace tree cell except that at least
24 one of a first plurality of transistors of said first Wallace tree
25 cell is constructed to have a width greater than a width of a

26 corresponding one a second plurality of transistors of said second
27 Wallace tree cell;

28 defining a first Booth decoder cell and a second Booth
29 decoder cell, each of said first Booth decoder cell structurally
30 the same as each of said second Booth decoder cell except that at
31 least one of a first plurality of transistors of said first Booth
32 decoder cell is constructed to have a width greater than a width of
33 a corresponding one of a second plurality of transistors of said
34 second Booth decoder cell;

35 disposing at least one first Wallace tree cell and at
36 least one first Booth decoder cell on said at least one critical
37 path;

38 disposing at least one second Wallace tree cell and at
39 least one second Booth decoder cell are on an electrical path not
40 said at least one critical path; and

41 not disposing any second Wallace tree cell or any second
42 Booth decoder on any of said at least one critical path.